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<u>L3</u>	L2 same ((host or cpu or operating or client or user) with (transparent or involv\$6 or action))	103	<u>L3</u>
<u>L2</u>	(request or command or read or write) near4 (combin\$4 or merg\$4 or consolidat\$3 or sort\$4)	11439	<u>L2</u>
<u>L1</u>	(request or command or read or write) near8 (combin\$4 or merg\$4 or consolidat\$3 or sort\$4)	16807	<u>L1</u>

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<u>L19</u>	scatter\$3 with gather\$3 with (disk or drive or disc)	69	<u>L19</u>
<u>L18</u>	\$gry not (angry or hungry)	349	<u>L18</u>
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<u>L16</u>	L15 and ((scatter adj2 list) or (data near4 pointer))	38	<u>L16</u>
<u>L15</u>	l14 and ((command adj2 block) or ((location or sector or track or address) near4 (ID or identif\$8)))	82	<u>L15</u>
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<u>L9</u>	((command or request) near4 ("same" or like or alike or similar or identical or relat\$3)) or read or write) near8 (buffer\$3 or queu\$4 or cach\$3)	45499	<u>L9</u>
<u>L8</u>	(disk or drive or disc) near8 (command or request or read or write)	68243	<u>L8</u>
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<u>L6</u>	L5 and ((command or request or read or write) near8 (concurrent\$3 or parallel or simultaneous\$2))	124	<u>L6</u>
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<u>L3</u>	l1 and ((queu\$4 or buffer\$3) with (read or write or command or request))	13186	<u>L3</u>
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	involv\$6 or action))		
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**1** [Run-time adaptation in river](#)

100%



Remzi H. Arpaci-Dusseau

ACM Transactions on Computer Systems (TOCS) February 2003

Volume 21 Issue 1

We present the design, implementation, and evaluation of run-time adaptation within the River dataflow programming environment. The goal of the River system is to provide adaptive mechanisms that allow database query-processing applications to cope with performance variations that are common in cluster platforms. We describe the system and its basic mechanisms, and carefully evaluate those mechanisms and their effectiveness. In our analysis, we answer four previously unanswered and important que ...

2 [Performance of the CRAY T3E multiprocessor](#)

100%



Ed Anderson , Jeff Brooks , Charles Grassl , Steve Scott

Proceedings of the 1997 ACM/IEEE conference on Supercomputing (CDROM)

November 1997

The CRAY T3E is a scalable shared-memory multiprocessor based on the DEC Alpha 21164 microprocessor. The system includes a number of novel architectural features designed to tolerate latency, enhance scalability, and deliver high performance on scientific and engineering codes. Included among these are **stream buffers**, which detect and prefetch down small-stride reference streams, **E-registers**, which provide latency hiding and non-unit-stride access capabilities, barrier and fetch_an ...

3 [User-space communication: a quantitative study](#)

100%



Soichiro Araki , Angelos Bilas , Cezary Dubnicki , Jan Edler , Koichi Konishi , James Philbin

Proceedings of the 1998 ACM/IEEE conference on Supercomputing (CDROM)

November 1998

Powerful commodity systems and networks offer a promising direction for high performance computing because they are inexpensive and they closely track technology progress. However, high, raw-hardware performance is rarely delivered to the end user. Previous work has shown that the bottleneck in these architectures is the overheads imposed by the software communication layer. To reduce these overheads, researchers have proposed a number of **user-space** communication models. The common featur ...

4 A CRT editing system

100%

4 Edgar T. Irons , Frans M. Djourup

Communications of the ACM January 1972

Volume 15 Issue 1

A text-editing and manipulation program is described. The program operates from low-cost cathode-ray tube entry and display stations with keyboard and 13 function buttons. Applications, potential economy of operation, and some aspects of implementation are discussed.

5 SPARK: a benchmark package for sparse computations

100%

4 Youcef Saad , Harry A. G. Wijshoff

ACM SIGARCH Computer Architecture News , Proceedings of the 4th international conference on Supercomputing June 1990

Volume 18 Issue 3

As the diversity of novel architectures expands rapidly there is a growing interest in studying the behavior of these architectures for computations arising in different applications. There has been significant efforts in evaluating the performance of supercomputers on typical dense computations, and several packages for this purpose have been developed, such as the Linpack benchmark, the Lawrence Livermore Loops, and the Los Alamos Kernels. On the other hand there has been little effort pu ...

6 Data relocation and prefetching for programs with large data sets

100%

4 Yoji Yamada , John Gyllenhall , Grant Haab , Wen-mei Hwu

Proceedings of the 27th annual international symposium on Microarchitecture November 1994

Numerical applications frequently contain nested loop structures that process large arrays of data. The execution of these loop structures often produces memory reference patterns that poorly utilize data caches. Limited associativity and cache capacity result in cache conflict misses. Also, non-unit stride access patterns can cause low utilization of cache lines. Data copying has been proposed and investigated in order to reduce cache conflict misses, but this technique has a high executio ...

7 Architecture: Leveraging cache coherence in active memory systems

99%

4 Daehyun Kim , Mainak Chaudhuri , Mark Heinrich


Proceedings of the 16th international conference on Supercomputing June 2002

Active memory systems help processors overcome the memory wall when applications exhibit poor cache behavior. They consist of either active memory elements that perform data parallel computations in the memory system itself, or an active memory controller that supports address re-mapping techniques that improve data locality. Both active memory approaches create coherence problems---even on uniprocessor systems---since there are either additional processors operating on the data directly, or the ...

- 8 Embedding Linux in a Commercial Product: A look at embedded systems and what it takes to build one 99%
Joel R. Williams
Linux Journal October 1999
- 9 ENWRICH: a compute-processor write caching scheme for parallel file systems 99%
Apratim Purakayastha , Carla Schlatter Ellis , David Kotz
Proceedings of the fourth workshop on I/O in parallel and distributed systems: part of the federated computing research conference May 1996
- 10 Comparison of Raw and Internet protocols in a HIPPI/ATM/SONET based gigabit network 99%
Raj K. Singh , Stephen G. Tell , Shaun J. Bharrat
ACM SIGCOMM Computer Communication Review January 1996
Volume 26 Issue 1
We compare implementation of Raw and Internet protocols (TCP, UDP) on a programmable HIPPI host-interface called the Network Interface Unit. The network interface unit connects Pixel-Planes 5, a message-based graphics multicomputer, to a wide area gigabit network called VISTAnet. The BISDN network consists of a SONET cross-connect switch and an ATM switch. We discuss the tradeoffs between protocols for our target application and present a comparison of end-to-end throughput based on empirical me ...
- 11 A faster UDP 99%
Craig Partridge , Stephen Pink
IEEE/ACM Transactions on Networking (TON) August 1993
Volume 1 Issue 4
- 12 Letters to the editor: Letters to the editor 99%
Communications of the ACM June 1964
Volume 7 Issue 6
- 13 Virtual database technology 99%
Ashish Gupta , Venky Harinarayan , Anand Rajaraman
ACM SIGMOD Record December 1997
Volume 26 Issue 4
- 14 Distributed storage control unit for the Hitachi S-3800 multivector supercomputer 99%
Katsuyoshi Kitai , Tadaaki Isobe , Tadayuki Sakakibara , Shigeko Yazawa , Yoshiko Tamaki , Teruo Tanaka , Kouichi Ishii
Proceedings of the 8th international conference on Supercomputing July 1994
This paper discusses the storage control unit of the Hitachi S-3800 supercomputer series, which is capable of achieving 8 GFLOPS in each of up to four shared-memory multiprocessors. This storage control unit is distributed to the V-SCs (vector-processor-side storage control units) and the M-SCs (main-storage-side storage control units), and achieves 128 gigabytes per second of total memory throughput. This distributed storage control unit supports scalability with increases in the number of ...

15 VMTP: a transport protocol for the next generation of communication systems

99%

 D Cheriton

Proceedings of the ACM SIGCOMM conference on Communications architectures & protocols September 1986

The Versatile Message Transaction Protocol (VMTP) is a transport-level protocol designed to support remote procedure call, multicast and real-time communication. The protocol is optimized for efficient page-level network file access in particular. In this paper, we describe the significant aspects of the VMTP design, including the VMTP treatment of sessions, addressing, duplicate suppression, flow control and retransmissions plus its provision for multicast. The VMTP design refle ...

16 Fast and flexible application-level networking on exokernel systems

98%

 Gregory R. Ganger , Dawson R. Engler , M. Frans Kaashoek , Héctor M. Briceño , Russell Hunt , Thomas Pinckney

ACM Transactions on Computer Systems (TOCS) February 2002

Volume 20 Issue 1

Application-level networking is a promising software organization for improving performance and functionality for important network services. The Xok/ExOS exokernel system includes application-level support for standard network services, while at the same time allowing application writers to specialize networking services. This paper describes how Xok/ExOS's kernel mechanisms and library operating system organization achieve this flexibility, and retrospectively shares our experiences an ...

17 Clustering: Evaluating document clustering for interactive information retrieval

98%

 Anton Leuski

Proceedings of the tenth international conference on Information and knowledge management October 2001

We consider the problem of organizing and browsing the top ranked portion of the documents returned by an information retrieval system. We study the effectiveness of a document organization in helping a user to locate the relevant material among the retrieved documents as quickly as possible. In this context we examine a set of clustering algorithms and experimentally show that a clustering of the retrieved documents can be significantly more effective than traditional ranked list approach. We a ...

18 Memory access scheduling

98%

 Scott Rixner , William J. Dally , Ujval J. Kapasi , Peter Mattson , John D. Owens


ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture May 2000

Volume 28 Issue 2

The bandwidth and latency of a memory system are strongly dependent on the manner in which accesses interact with the "3-D" structure of banks, rows, and columns characteristic of contemporary DRAM chips. There is nearly an order of magnitude difference in bandwidth between successive references to different columns within a row and different rows within a bank. This paper introduces memory access scheduling, a technique that improves the performance of ...

19 Exploiting ILP in page-based intelligent memory

98%

 Mark Oskin , Justin Hensley , Diana Keen , Frederic T. Chong , Matthew Farrens , Aneet

Chopra

**Proceedings of the 32nd annual ACM/IEEE international symposium on
Microarchitecture** November 1999

This study compares the speed, area, and power of different implementations of Active Pages [OCS98], an intelligent memory system which helps bridge the growing gap between processor and memory performance by associating simple functions with each page of data. Previous investigations have shown up to 1000X speedups using a block of reconfigurable logic to implement these functions next to each sub-array on a DRAM chip. In this study, we show that instruction-level parallelism, n ...

20 Disco: running commodity operating systems on scalable multiprocessors



98%

 Edouard Bugnion , Scott Devine , Kinshuk Govil , Mendel Rosenblum

ACM Transactions on Computer Systems (TOCS) November 1997
Volume 15 Issue 4

In this article we examine the problem of extending modern operating systems to run efficiently on large-scale shared-memory multiprocessors without a large implementation effort. Our approach brings back an idea popular in the 1970s: virtual machine monitors. We use virtual machines to run multiple commodity operating systems on a scalable multiprocessor. This solution addresses many of the challenges facing the system software for these machines. We demonstrate our approach with a prototy ...

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